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☐	L29	(head near5 pointer) and (tail near5 pointer$1)	1624
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☐	L21	L20 and (empty near5 queue)	30
☐	L20	L19 and queue	33
☐	L19	L18 and dequeue	33
☐	L18	L17 and (head near5 tail)	33
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☐	L16	L15 and descriptor	51
☐	L15	L14 and (queue same dequeue)	95
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☐	L12	5671446.uref.	14
☐	L11	(memory near5 head) same (queue near5 enqueue)	12
☐	L10	L7 and (head near5 point$)	10
☐	L9	L7 and (dequeue$1)	2
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☐	L5	'memory enqueue'.ti.	0
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☐   L4   EP-1478142-A2.did.   0

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In normal chaining mode, message **descriptors** are used to contain all the information
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The **queue** con-sists of an array of buffer **descriptors**, a **head pointer**, ...
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event in the process' event **queue**, but this may be hundreds ... copies of the
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Multiple DMA **descriptors** per packet. Should not under-utilize available link ...
Each **queue** is represented as a linked list with **head/tail**/next **pointers** ...
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ing allows each process to maintain a local work **queue**, and ... a new PCB and
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EPICURE Design Note 3.9<P> VMS System Services for QVI Support
The **head pointer** is the CM offset (from the base of Common Memory) to the ...
The **tail pointer** is the CM offset to the last **(tail)** entry on the **queue** (of 0 ...
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[PS] A Scalable Architecture for Fair Leaky-Bucket Shaping Jennifer ...
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Although this requires additional memory to store a **pointer** field with each cell,
... where each list consists of a **head pointer**, a **tail pointer**, ...
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Summary of changes from v2.5.75 to v2.6.0-test1 ...
However, due to relaxed memory ordering model, the **tail pointer** can be visible
before the actual event is ... It is using local variable as wait **queue head**. ...
www.kernel.org/pub/linux/kernel/ v2.6/pre-releases/ChangeLog-2.6.0-test1 - 39k - Cached - Similar pages

On Network CoProcessors for Scalable, Predictable Media Services
... buffer is maintained for each stream, with separate **head** and **tail pointers**.
... Table 1 records microbenchmarks for both a software floating-**point** ...

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In fact, these shadow registers are part of a **queue** of **descriptors** which contain
... Launch packet; this Idio returns the **head pointer** for. the DMA channel. ...
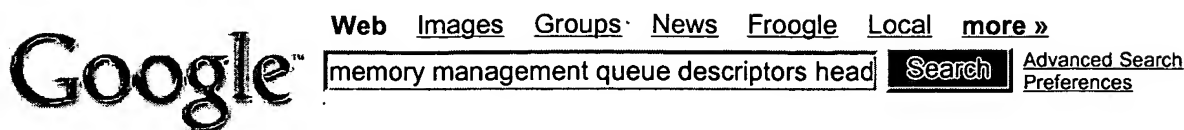www.lcs.mit.edu/pubs/pdf/MIT-LCS-TM-503.pdf - Similar pages

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[PPT] Computer Hardware Review
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Pointers to scheduling queues. **Memory Management** Information ... Each device has
its own device **queue**. 16. **head. tail. head. tail. head. tail. head. tail** ...
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entry of a **queue**), the **tail pointer** (address of the last entry. of a **queue**), and
a count entry ... return **queue descriptors** to **memory** and fetch new **queue** ...
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[PDF] High Performance RDMA-Based MPI Implementation over InfiniBand
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for a sender when the **head pointer** meets the **tail pointer**. At the sender side,
the **head** ... lated to the **management** of **descriptors** and buffers. First, ...
nowlab.cse.ohio-state.edu/ projects/mpi-iba/publication/ics03.pdf - Similar pages

CS 564 Project Part 1: Buffer Manager
Finally, return a **pointer** to the page (in the buffer pool) by reference. ...
We also must keep **head** and **tail pointers** to indicate the two ends of the **queue**. ...
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RDMA **descriptors**. A descriptor contains both the local ... in shared **memory**,
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memory management is provided [4, 7]. Alternately, in. Section 2.2 we provide a
simple dynamic ... a new PCB and initializes its **head** and **tail pointers** to ...
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[PDF] Application Notes 8.19:USB97C102 Programmers Reference Guide - SMSC
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At the center of the device is a multi-ported MMU (**Memory Management** Unit) ...
When each **queue** is empty, its **head** and **tail pointers** are equal; a **queue** is ...
www.smsc.com/main/anpdf/an819.pdf - Similar pages

[PDF] PA-4R-DTR Dedicated Token Ring Port Adapter
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To display information about **memory management**, error counters, the CSC-IR, ...
Descriptors outstanding (curr/max): 0/256. **Head pointer**: 7 **Tail pointer**: 7 ...
www.cisco.com/univercd/cc/td/doc/ product/software/ios113ed/113t/113t_3/pa4rdtr2.pdf - Similar pages

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and finally in line 18 it tries to swing the **head pointer** (ie,. Anchor.avail)
atomically to the ... algorithm in [20] with optimized **memory management** for ...
www.cs.utah.edu/~wilson/ compilers/papers/pldi04-michael.pdf - <u>Similar pages</u>

[PDF] Incorporating **Memory Management** into User-Level Network Interfaces
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The work presented here addresses the **memory management** issues on commodity
processors **...** tor onto the send **queue**. The descriptor contains **pointers** to the **...**
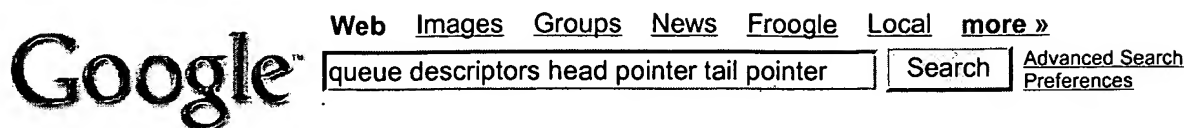www.cs.cornell.edu/tve/u-net/papers/unetmm.pdf - <u>Similar pages</u>

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<u>Exercises 6: Linked-List **Queue** Management (U.Crete, F'01, CS-534)</u>
6.1 **Pointer**-Access Cost of Enqueue and Dequeue Operations ... in the latter case,
we can store one **head** or **tail pointer** plus one Empty Flag in one word of ...
archvlsi.ics.forth.gr/~kateveni/534/01f/exer06.html - 10k - <u>Cached</u> - <u>Similar pages</u>

<u>Exercises 5: Multi-Packet Blocks, Multicast Queues (U.Crete, CS-534)</u>
The **head** and **tail pointers** of each **queue**, on the other hand, ... (b) Now consider
the second scheme --**queue**-member **descriptors** that are decoupled from ...
archvlsi.ics.forth.gr/~kateveni/534/05a/ex05_advq.html - 9k - <u>Cached</u> - <u>Similar pages</u>

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described in Work **Queue** Requests (WQR), or **descriptors**,. and submitted to the
work **queue**. ... for a sender when the **head pointer** meets the **tail pointer**. ...
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queue request has been finished. InfiniBand also supports ... in shared memory,
together with a **head pointer** and a **tail. pointer**. The put operation copies ...
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<u>CSCI 320</u>
Insert the element pointed to by p into the **queue** whose **tail-pointer** is pointed
... Return a **pointer** to the process table entry that is at the **head** of the ...
cerebro.xu.edu/csci320/99f/ Assignments/TINA-phase1/phase1-3.html - 15k - <u>Cached</u> - <u>Similar pages</u>

[PDF] <u>A Scalable, Cache-Based **Queue** Management Subsystem for Network ...</u>
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Both the **queue descriptors**, consisting of **head** and **tail. pointers** and the **queue**
length, ... **tail point** to the new **tail**. 4. Write back the updated **queue**. ...
www.arl.wustl.edu/~pcrowley/beacon.pcrowley.pdf - <u>Similar pages</u>

<u>PA-4R-DTR Dedicated Token Ring Port Adapter</u>
... **pointer**: 7 **Tail pointer**: 7 Receive ring: Ring size: 64 **descriptors Head pointer**:
... Each number is followed by a slash, the maximum size of the **queue**, ...
www.cisco.com/univercd/cc/td/doc/ product/software/ios113ed/113t/113t_3/pa4rdtr2.htm - 41k -
<u>Cached</u> - <u>Similar pages</u>

[PDF] <u>Intel Technology Journal</u>
File Format: PDF/Adobe Acrobat - <u>View as HTML</u>
The data store for each **queue**. descriptor contains the **head pointer** (address of
the first. entry of a **queue**), the **tail pointer** (address of the last entry ...
www.intel.com/technology/itj/2002/ volume06issue03/art01_nextgenixp/vol6iss3_art01.pdf - <u>Similar pages</u>

<u>EPICURE Design Note 6.3<P> <b> Use of the QVI and Common VME ...</u>
A CM **queue** is a singly-linked FIFO list. The **head pointer** is the ... The **tail**
pointer is the CM-**pointer** to the last (**tail**) entry on the **queue** (or 0 if the ...
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